Remarks

Reconsideration is respectfully requested.

Claims 1-22 were originally pending in this application.

Independent claims 1, 11, 21, and 22 are amended. Dependent claims 7 and 8 are also amended.

In brief, the invention is specialized test software operating on an embedded processor that creates one or more test workers or threads, each having a specific routine to perform, which are executed in parallel, stressing various communication paths. The results may be analyzed to help in many different ways during the life cycle of a device containing the embedded processor.

The test software is a standardized test suite that is capable of exercising all of the input and output ports of an embedded processor, regardless if those input and output ports are used in a specific application. The test software may be preconfigured to exercise each of the input and output ports in various manners so that when powered up and operating, an engineer may diagnose and debug the circuitry of the device using standardized test software. The standardized test software may be reused for every board design or application that uses the embedded processor, and may greatly reduce the time required to 'turn on' a new circuit design.

Finality of Previous Office Action Is Improper

In the Office action dated 15 Nov 2007, the explanation of a rejection for Independent Claims 11 and 21 were omitted.

Applicant requested that any further rejection of unchanged claim 21 would have to be a non-final Office action. MPEP 706.07(a). The Examiner reminded the Applicant of "their duty to fully read the references provided by the Examiner and therefore a new non-Final action will not be granted".

From MPEP 2142: "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness."

Since the Examiner did not factually support a prima facie case in the first Office action, Applicant was unable to formulate a response. By making the Office action of 26 Jun 2008 a Final Office action, Applicant has not been afforded his opportunity to have his case fully considered by the Office.

Applicant respectfully requests that the Finality of the previous Office action be withdrawn and that this Amendment be fully considered. See MPEP 706.07(a).

Amendments to the Claims

Claim 1 is amended to include "at least one performance parameter". Support for the amendment may be found, among other places, at line 3 of page 7 of the specification. Claim 8 is similarly amended.

Claims 11, 21, and 22 are amended to include parallel threads that may operate on a single port. Support for the amendments may be found, among other places, at line 7 of page 2 of the specification. Claim 7 is similarly amended.

35 USC §112 Rejections

Claims 1-20 and 23 are rejected under 35 USC 112 as failing to comply with the written description requirement. Without admitting or arguing the appropriateness of the rejection, Applicant has amended independent claims 1, 11, and 23 to remove references to 'fewer number of input ports and the embedded processor', rendering the rejection moot.

35 USC §102(e) Rejections

Claim 21 is rejected under 35 USC 102(e) as being anticipated by DeRolf (US Pat 6,904,544).

Applicant thanks the Examiner for explaining the rejection of independent claim 21 and allowing the Applicant an opportunity to respond.

The rejection is respectfully traversed for at least the following reasons.

The amendment to claim 21 recites a first embedded processor being in a first circuit having a first functionality, and a second embedded processor being in a second circuit having a second functionality, the second functionality being different from the first functionality.

Neither DeRolf nor any reference of record mentions having two different applications for a single, reusable test sequence. DeRolf only describes and application of testing a Storage Area Network, for example, but does not describe using a reusable test sequence with another processor having a different functionality.

It is well-established law that, for a proper rejection of a claim under 35 U.S.C. § 103 (or 35 U.S.C. § 102) as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all elements, features, or steps of the claim at issue. See, e.g., *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). *Glaverbel S.A. v. Northlake Mkt'g & Supp., Inc.*, 45 F.3d 1550, 33 USPQ 2d 1496 (Fed. Cir. 1995) ("the claimed process, including *each step* thereof, *must have been described* or embodied, either *expressly or inherently*.") (Emphasis added.) As clearly articulated in M.P.E.P. § 2143.03, "[to] establish *prima facie* obviousness of a claimed invention, *all the claim limitations must be taught or suggested* by the prior art." *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). "*All words* in a claim *must be considered in judging the patentability* of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (C.C.P.A. 1970). (Emphasis added.)

(1) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach a reusable test sequence as claimed in independent claim 21.

DeRolf does not teach of a 'reusable' test sequence. 'Reusable' is often defined as "to use something again, often for a different purpose". DeRolf's test sequence is limited in scope only to testing Storage Area Networks.

(2) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach a command interpreter as claimed in independent claim 21.

A command interpreter is not described or even mentioned in DeRolf, let alone two instances of a command interpreter as required by the claims.

In the cited reference of Column 3, Lines 40-50, DeRolf uses a 'state machine'. From Wikipedia, "A finite state machine (FSM) or finite state automaton (plural: automata) or simply a state machine, is a model of behavior composed of a finite number of states, transitions between those states, and actions." (http://en.wikipedia.org/wiki/State_machine viewed 14 Aug 2008).

This is in stark comparison to a 'command interpreter', which is defined in Wikipedia as "A command line interpreter (also command line shell, command language interpreter) is a computer program that reads lines of text entered by a user and interprets them in the context of a given operating system or programming language." (http://en.wikipedia.org/wiki/Command_interpreter viewed 14 Aug 2008).

The 'state machine' of DeRolf is not equivalent to the 'command interpreter' as claimed. One of the reasons why a 'command interpreter' is claimed is that the test system may be reused in many different applications. By constructing the test system as a command interpreter, the test system may have much more flexibility, configurability, and reusability and a state machine architecture.

(3) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "outputting results" as claimed in independent claim 21.

In the cited reference of Column 11, Lines 20-30, DeRolf describes "verbose command causes the state machine to display all messages to a screen display". DeRolf does not state that the 'messages' were results of a test. In fact, DeRolf does not describe displaying any results in any manner.

See Column 11, Lines 40-41, where DeRolf describes an 'interactive' mode:

> interactive: instructs the state machine 102 to allow the user to interact with the state machine to perform manual fault isolation. This arrangement causes the state machine to instruct the administrator to plug and unplug components as the rules evaluate the results to determine the faulty FRU. (Emphasis added).

DeRolf does not describe 'outputting results' as required in the claims. The claims require a specific type of information to be displayed, namely 'results' that were obtained from analysis of timestamps. DeRolf does not describe 'outputting results' of any fashion that may be derived from any test whatsoever. The Examiner's explanation in the Response to Arguments section does not reconcile the deficiencies of DeRolf.

(4) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "timestamping on outgoing message" and "timestamping an incoming message" as claimed in independent claim 21.

The Office cites Column 11, Line 45-55 as being equivalent. DeRolf at that citation reads:

> Once the expert diagnostic tool 100 is invoked with the above arguments, the state machine 102 records a start record with a timestamp into the activity log and processes the rule base completely for each specified disk. When the state machine encounters the end of the rule base, it records the state of the tested storage path as COMPLETED or FAILED. If FAILED, the activity log records the name of the loges) that contain failed test data, such as the suspect list 112. These error log files contain important information that should accompany the failed component(s) back to the 55 repair station, such as the suspect list 112 that indicates components that may be the source of the failure. (Emphasis added).

DeRolf only describes timestamping a start time, then processes the rule base completely before timestamping at the end of the rule base. DeRolf as cited does not describe timestamping individual messages that are sent and received as required in the claims.

Claim 22 is rejected under 35 USC 102(e) as being anticipated by Oberlaender (US PGPUB 2005/0102572).

The rejection is respectfully traversed for at least the following reasons.

The amendment to claim 22 recites at least two threads configured to operate in parallel on a single port.

Neither Oberlaender, DeRolf, nor any reference of record mentions having two threads operating in parallel on a single port. The operation of two or more threads on a single port may

enable the full bandwidth of the port to be used up, which may enable various performance measurements.

(1) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach assembling a circuit as claimed in independent claim 22.

Oberlaender does not actually teach of assembling a circuit, but only of fabricating a single integrated circuit device in paragraph [0003]. In order to 'assemble', one must take two or more distinct pieces and join them together. This differs from the manufacture of integrated circuits where various layers are built up as defined in masks.

The distinction between 'assembling' a circuit as claimed and the fabrication of a circuit of Oberlaender highlights some of the differences between the claimed invention and the cited prior art. The claimed invention describes method for developing a circuit, such as a circuit on a printed circuit board, where an embedded processor may be loaded with a test sequence that fully exercises the circuitry.

The Office further cites paragraph [0025] and states "it is here that Oberlaender teaches that the simulation model includes a processor core that can process program instructions that are associated with test programs and data file that are stored in the memory array. Later on Oberlaender mentions that separate program and data memory devices may be used. Therefore, Oberlaender does teach software operable on said embedded processor."

Applicant respectfully asserts that this citation teaches away from the claimed invention as interpreted by the Examiner. The claimed invention requires that the test software operate on the embedded processor, not an external or host processor.

(2) Oberlaender is non-analogous art and does not teach of operating a processor as claimed. Oberlaender only teaches of simulating a processor, not executing an actual processor in an actual circuit as claimed.

The development and testing of integrated circuits is non analogous art in many aspects. In integrated circuits, the circuit paths are verified and thoroughly tested using simulation tools and other mechanisms. After manufacture, any testing is directed toward ensuring that the manufactured product corresponds with the designed circuitry. In most cases, the designer may only change the circuit by changing the design, performing the simulation methods, and

manufacturing a new version. For an integrated circuit, almost all of the circuit design, testing, and analysis is performed before manufacture.

In the development and testing method of the claimed invention, a designer may use breadboarding, printed circuits, or other methods to connect various components. In some cases, no circuit simulation may be performed before assembly. Such an environment can benefit from a much more comprehensive, versatile, and interactive circuit testing mechanism such as the claimed invention.

Part of the claimed invention is that the testing mechanism be operable on the embedded processor itself, not from a host device or from a separate processor. The test system operating on the embedded processor greatly reduces the debugging time of the overall circuit, which may include printed circuit boards, components, breadboards, and other components and connections. This is because the test signals originate on the embedded processor, as opposed to being sent from an external source. Oberlaender does not generate test signals on an embedded processor and cannot be used to solve the problem addressed by the claimed invention.

Tools for designing and testing integrated circuits, such as Oberlaender, are used for a different purpose and operate on theoretical or simulated circuits, and are therefore non-analogous to the claimed invention.

Oberlaender only teaches of simulating a circuit using a simulated processor, not an actual processor as claimed. See Oberlaender at line 9 of paragraph [0009]: "The method begins by loading a set of initial data values into the memory circuit of a simulated SOC design (i.e., the simulation model). Simulated execution of a test program by the simulation model is then performed using known techniques. To chronical (sic) memory changes (e.g., data write operations), address and data signals transferred to memory interfaces associated with the simulated model are utilized to form incremental transaction records." (Emphasis added).

Operlaender does not teach of using an 'embedded processor', but only a 'simulated' processor.

(3) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "a command interface" as claimed in independent claim 22.

As claimed, the 'command interface' is 'adapted to receiving commands and outputting results'. The Office cites Oberlaender's 'interface circuit' as described in paragraph [0027] as equivalent.

Oberlaender's 'interface circuit' is item 222. From paragraph [0025] of Oberlaender: "In addition, memory array 220 includes an interface circuit 222 that communicates with CPU pipeline 210 over system bus 215, an array of memory cells 226, and a memory control unit (MCU) 224 coupled between interface circuit 222 and memory cells 226." Oberlaender's 'interface circuit' is not 'adapted to receiving commands and outputting results' as claimed, but only serves to connect different components within a simulated circuit.

(4) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "timestamping outgoing messages and storing said messages" as claimed in independent claim 22.

Outgoing and incoming messages as described in the specification, are messages sent through input and output ports on a device with an embedded processor.

The Office cites Oberlaender's 'timestamp values' as equivalent. Oberlaender discusses timestamping only in the context of recognizing a change in a simulated memory device and storing the memory information with a time stamp.

The cited reference includes: "To chronical (sic) simulated accesses to memory array 220 (e.g., simulated data write operations), address and data signals transferred to interface circuit 222 are captured by memory tracer 234, which then generates incremental transaction records that are stored in transaction record storage region 236 (block 340). As described in additional detail below, each transaction record includes a timestamp value indicating when the transaction occured, address information identifying, for example, the memory cells changed during a write operation, the actual data written to these memory cells, and, an optional data field indicating an access width (i.e., amount of the accessed/written data)." The "transaction record" is not equivalent to a "message" as claimed.

Oberlaender does not teach of timestamping incoming or outgoing messages as required in the claims.

(5) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "displaying the results" as claimed in independent claim 22.

The Office cites Oberlaender at paragraph [0063] and specifically the sentence "Data is typically written to fifo devices using "push" or "push write" operations, and is read removed) from the fifo device using "pop" operations." The Office provides no further explanation as to why this sentence has anything to do with "displaying the results" as claimed.

Absent any explanation by the Office, Applicant asserts that "displaying the results" of a performance test has nothing to do with the operation of FIFO devices.

(6) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "transmitting a test sequence to an embedded processor" as claimed in independent claim 22.

The Office cites Oberlaender at paragraph [0048] as being equivalent, specifically a "...parallel shows the transaction stream...". In paragraph [0048], Oberlaender discusses a GUI 238 (Graphical User Interface) that "displays the instantaneous data values stored in the memory array, and in parallel shows the transaction stream leading up to the instantaneous memory content (i.e., one or more transaction records associated with the displayed instantaneous data values)." Oberlaender goes on to state that an exemplary representation is shown in Figure 7.

In paragraph [0048] and Figure 7, Oberlaender does not teach nor even mention 'transmitting a test sequence to an embedded processor'. Oberlaender only discusses a user interface that may show transaction records and values in a memory array.

The claims require that a test sequence be 'transmitted to an embedded processor'. The Office has failed to cite any transmission and further failed to cite any embedded processor as required in claim 22.

Claim 23 is rejected under 35 USC 102(e) as being anticipated by Toth (US Pat 4,829,520).

The rejection is respectfully traversed for at least the following reasons.

The amendment to claim 23 recites at least two threads configured to operate in parallel on a single port.

Neither Oberlaender, DeRolf, nor any reference of record mentions having two threads operating in parallel on a single port. The operation of two or more threads on a single port may enable the full bandwidth of the port to be used up, which may enable various performance

35 USC §103 Rejections

Claims 1-7, 9 and 10 are rejected under 35 USC 103(a) as being anticipated by DeRolf in view of Toth.

The rejection is respectfully traversed for at least the following reasons.

As stated in the Manual of Patent Examining Procedure at section 2141:

Office Personnel As Factfinders

Office personnel fulfill the critical role of factfinder when resolving the Graham inquiries. It must be remembered that while the ultimate determination of obviousness is a legal conclusion, the underlying Graham inquiries are factual. When making an obviousness rejection, Office personnel must therefore ensure that the written record includes findings of fact concerning the state of the art and the teachings of the references applied. In certain circumstances, it may also be important to include explicit findings as to how a person of ordinary skill would have understood prior art teachings, or what a person of ordinary skill would have known or could have done. Factual findings made by Office personnel are the necessary underpinnings to establish obviousness.

Once the findings of fact are articulated, Office personnel must provide an explanation to support an obviousness rejection under 35 U.S.C. 103. 35 U.S.C. 132 requires that the applicant be notified of the reasons for the rejection of the claim so that he or she can decide how best to proceed. Clearly setting forth findings of fact and the rationale(s) to

support a rejection in an Office action leads to the prompt resolution of issues pertinent to patentability.

In short, the focus when making a determination of obviousness should be on what a person of ordinary skill in the pertinent art would have known at the time of the invention, and on what such a person would have reasonably expected to have been able to do in view of that knowledge. This is so regardless of whether the source of that knowledge and ability was documentary prior art, general knowledge in the art, or common sense.

It is well-established law that, for a proper rejection of a claim under 35 U.S.C. § 103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all elements, features, or steps of the claim at issue. See, e.g., *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). *Glaverbel S.A. v. Northlake Mkt'g & Supp., Inc.*, 45 F.3d 1550, 33 USPQ 2d 1496 (Fed. Cir. 1995) ("the claimed process, including *each step* thereof, *must have been described* or embodied, either *expressly or inherently*.") (Emphasis added.) As clearly articulated in M.P.E.P. § 2143.03, "[to] establish *prima facie* obviousness of a claimed invention, *all the claim limitations must be taught or suggested* by the prior art." *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). "*All words* in a claim *must be considered in judging the patentability* of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (C.C.P.A. 1970). (Emphasis added.)

The Supreme Court of the United States and the Court of Appeals for the Federal Circuit have provided further guidance for resolving the question of obviousness. "An obviousness determination is *not the result of a rigid formula* disassociated from the consideration of the facts of a case. Indeed, the common sense of those skilled in the art demonstrates why some combinations would have been obvious where others would not." See *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1739, 167 L.Ed.2d 705 (2007). *Leapfrog Ent., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 82 USPQ2d 1687 (Fed. Cir. 2007). (Emphasis added.)

In *KSR, supra*, the Supreme Court articulated guidelines for determining obviousness. One of the guidelines is that there is some benefit from the proposed modification. ("A person

having ordinary skill in the art could have combined Asano with a ... sensor ..., and *would have seen the benefit* of doing so." *Id.* at 1743 (Emphasis added). "The proper question to have asked was whether ... [a person] of ordinary skill [in the art] ... *would have seen a benefit to upgrading* Asano with a sensor." *Id.* at 1743 (Emphasis added).)

"Although common sense directs caution as to a patent application claiming as innovation the combination of two known devices according to their established functions, *it can be important to identify a reason that would have prompted a person of ordinary skill in the art to combine the elements as the new invention does.* Inventions usually rely upon building blocks long since uncovered, and claimed discoveries almost necessarily will be combinations of what, in some sense, is already known." *Id.* at 1731 (Emphasis added).

In *KSR, supra*, the Supreme Court noted that it will be necessary for a court "to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be explicit." *KSR Intern. Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741, 1746 (2007). *"[R]ejections* on obviousness grounds *cannot be sustained by mere conclusory statements;* instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.* at 1746, quoting *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006). (Emphasis added.)

In decisions decided after *KSR, supra*, the Board of Patent Appeals and Interferences has failed to sustain obviousness type rejections when the examiner has failed to make a proper *prima facie* case of obviousness. See *Ex parte Katoh et al*, Appeal 2007-1460 (obviousness rejection not sustained because there was "no evidence or suggestion" in the reference for the alleged configuration); and *Ex parte Crawford et al*, Appeal 2006-2429 (obviousness rejection not sustained because there was no suggestion to combine the references in the manner suggest by the examiner except for using the Appellants' invention as a template through hindsight reconstruction of Appellants' claims).

(1) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "timestamping on outgoing message" and "timestamping an incoming message" as claimed in independent claim 1.

Applicant's argument discussed above for a similar limitation to claim 21 also applies to claim 1. The argument is not included here for brevity, but is included by reference.

(2) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "a test sequence comprising multiple threads of commands" as claimed in dependent claims 6 and 16.

The Office cites column 3, lines 59-67 of DeRolf as being equivalent. The Office further cites column 11, lines 20-35 and column 12, lines 20-33 as showing "multiple threads".

DeRolf, in the cited reference or in any location, does not describe a 'test sequence having multiple threads of commands'. As defined in Wikipedia:

> A thread in computer science is short for a thread of execution. Threads are a way for a program to fork (or split) itself into two or more simultaneously (or pseudo-simultaneously) running tasks. Threads and processes differ from one operating system to another but, in general, a thread is contained inside a process and different threads in the same process share some resources while different processes do not. (http://en.wikipedia.org/wiki/Thread_%28computer_science%29 viewed 14 Aug 2008).

DeRolf does not mention threads in any place whatsoever, and Toth does not overcome the deficiency of DeRolf.

As explained above, DeRolf uses a state machine which is not a multithreaded interpreter, which would be required as claimed. In addition to the fact that DeRolf does not in any manner describe multiple threads, it would be technically impossible to have a test sequence comprising multiple threads of commands using a state machine as taught by DeRolf.

The claims require threads and specifically multiple threads. DeRolf does not specifically mention threads, thread based architectures, or any other technology that may be construed as containing threads. While DeRolf does attempt an omnibus statement in column 12, lines 20-33, all of DeRolf's various embodiments relate to different descriptors for functions (column 12, lines 20-26), different methods for user interface interaction (column 12, lines 27-32), and different architectures for Storage Area Networks (column 12, lines 33-40). DeRolf does not, in any manner, describe different architectures for the test mechanism other than the state machine.

(3) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "input driver adapted to validate an incoming message" as claimed in dependent claim 7.

The Office cites DeRolf at column 13, lines 15-20 "a device interface". The citation states a 'device interface', but does not attribute any specific functionality to the 'device interface'. Specifically, the claim requires that the 'input driver be adapted to validate an incoming message'. The Office has not shown where the 'device interface' validates an incoming message, nor has the Office explained where such a feature may be attributed.

(4) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "an initiator adapted to determine if an I/O device is present" as claimed in dependent claim 7.

The Office cites DeRolf at column 13, lines 15-20 "a device interface". The citation states a 'device interface', but does not attribute any specific functionality to the 'device interface'. Specifically, the claim requires that the "an initiator adapted to determine if an I/O device is present". The Office has not shown where the 'device interface' validates an incoming message, nor has the Office explained where such a feature may be attributed.

(5) The Office has not met its burden under M.P.E.P. § 2143.03 to show cited combination of references that teach "an input driver further adapted to validate an incoming message" as claimed in dependent claim 17.

The Office cites DeRolf at column 13, lines 15-20 "a device interface". The citation states a 'device interface', but does not attribute any specific functionality to the 'device interface'. Specifically, the claim requires that the "an input driver further adapted to validate an incoming message". The Office has not shown where the 'device interface' validates an incoming message, nor has the Office explained where such a feature may be attributed.

Applicant believes no new material has been added. Applicant invites the Examiner to call the undersigned at 970-690-4023 to suggest any changes or discuss any actions so that this case may be quickly allowed.

The applicant believes the application to be in condition for allowance, and such action is earnestly requested.

Dated this 19th day of August, 2008.

Respectfully submitted:

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